USN | | | | | | | | | | |

15EC46

Fourth Semester B.E. Degree Examination, June/July 2018
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note:1. ***Answer FIVE full questions, choosing one full question from each module.***
2. Use of standard resistor value and standard capacitor value table is allowed.

Module-1

1 a. With neat circuit diagram, explain basic op-amp circuit. **(06 Marks)**

b. Sketch an op-amp difference amplifier circuit. Derive an equation for output voltage and explain the operation. **(05 Marks)**

c. A non inverting amplifier is to amplify a 100 mV signal to a level of 3 V. Using 741 op-amp design a suitable circuit. **(05 Marks)**

OR

2 a. Define following terms with respect to op-amp and mention their typical values:
(i) PSRR (ii) CMRR (iii) Slew rate. **(06 Marks)**

b. With neat circuit diagram, explain the operation of a direct coupled inverting amplifier with necessary design steps. **(04 Marks)**

c. Obtain the expression for the three input inverting summing amplifier circuit and show how it can be converted into averaging circuit. **(06 Marks)**

Module-2

3 a. Sketch and explain high zin capacitor coupled voltage follower with necessary design steps and show that the input impedance is very high as compared to capacitor coupled voltage follower. **(08 Marks)**

b. What are the advantages of precision rectifier over ordinary rectifier? Discuss the operation of precision full wave rectifier circuit using bipolar op-amp. **(08 Marks)**

OR

4 a. Draw the circuit diagram of instrumentation amplifier and explain its operation. Also show how voltage gain can be varied. **(08 Marks)**

b. A capacitor coupled non-inverting amplifier is to have $A_V = 100$ and $V_0 = 5$ V with $R_L = 10$ KΩ and $f_l = 100$ Hz. Design a suitable circuit using 741 op-amp. **(08 Marks)**

Module-3

5 a. Draw and explain the operation of sample and hold circuit with signal, control and output waveforms. **(08 Marks)**

b. Using 741 op-amp with a supply of ±12V, design a phase shift oscillator to have an output frequency of 3.5 kHz and voltage gain of 29. ($A_V = 29$) **(08 Marks)**

OR

6 a. With neat circuit diagram explain the working of precision clipping circuit, with necessary waveforms. **(08 Marks)**

b. With neat circuit diagram, explain the operation of inverting Schmitt trigger circuit. Draw the output waveforms and discuss the design procedure. **(08 Marks)**

Module-4

7 a. Draw the internal schematic for 723 IC low voltage regulator and explain its working and also mention the advantages of IC voltage regulators. **(08 Marks)**

b. Design and explain the operation of second order active low pass filter. Using 741 op-amp to have a cut-off frequency of 2 kHz. **(08 Marks)**

OR

8 a. Show how a band pass filter can be constructed by the use of a low pass filter and a high pass filter. Sketch the expected frequency response and explain the operation of a single stage Band Pass Filter. **(08 Marks)**

b. Discuss the important characteristics of a three terminal IC regulator and design a 7805 IC regulator to get the output voltage of 7.5 V (Choose $I_Q = 4.2$ mA, $I_{R_1} = 25$ mA) **(08 Marks)**

Module-5

9 a. With the help of neat block diagram, explain the operation of Phase – Locked Loop (PLL) and define

(i) Lock-in range (ii) Capture range (iii) Pull-in time **(08 Marks)**

b. Explain the working of successive approximation Analog-to Digital Converter (ADC). **(08 Marks)**

OR

10 a. Draw the internal schematic of 555 timer IC and configure it for monostable operation and explain its working with necessary equations. **(08 Marks)**

b. Explain the working of R-2R network D-A converter and derive expression for output voltage. **(08 Marks)**

* * * * *

CBCS Scheme

USN | | | | | | | | | | |

15EC46

Fourth Semester B.E. Degree Examination, Dec.2017/Jan.2018

Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing one full question from each module.

Module-1

1 a. Define following terms with respect to opamp and mention the typical values of opamp 741: (i) PSRR, (ii) CMRR, (iii) Slew rate, (iv) input voltage range and output voltage range. **(08 Marks)**

b. Compare emitter follower with voltage follower. **(04 Marks)**

c. A voltage follower using 741 opamp is connected to signal source with resistance of R_s = 47 KΩ. Calculate suitable value of resistor R_1 and also maximum voltage drop across each resistor and maximum input offset voltage produced by input offset current.

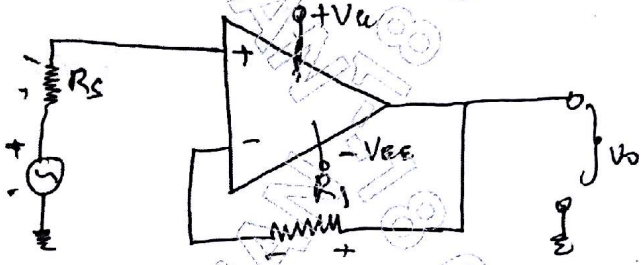

Fig.Q1(c) **(04 Marks)**

OR

2 a. Derive output voltage equation of 3 input non inverting summing circuit and show how it can be converted into averaging circuit. **(08 Marks)**

b. An operational amplifier circuit with closed loop gain is 100 and common mode output voltage is 5 mV and common mode input is 5 mV, determine common mode rejection ratio. **(02 Marks)**

c. Explain the operation of a basic op-amp circuit. **(06 Marks)**

Module-2

3 a. Explain capacitor coupled voltage follower circuit. **(08 Marks)**

b. Design a precision voltage source to provide an output of 9 V the available supply is ±12V allow approximately ±10% tolerance on Zener diode voltage. **(08 Marks)**

OR

4 a. Design an instrumentation amplifier to have an overall gain of 900. The input signal amplitude of 15 mV, 741 opamp is to be used. Supply is ±15V. **(08 Marks)**

b. Explain high Zin capacitor coupled non inverting amplifier with design steps. **(08 Marks)**

Module-3

5 a. Explain precision clipping circuit. **(08 Marks)**

b. Explain log amplifier and derive its output voltage equation. **(08 Marks)**

OR

6 a. Using 741 opamp with supply voltage of ±12V design Schmitt trigger to have trigger points ±2V. **(06 Marks)**

b. Explain sample and hold circuit using of opamp. **(10 Marks)**

Module-4

7 a. Explain second order active low pass filter and also write design equations. **(08 Marks)**

b. Explain the function diagram of 723 general purpose regulator IC. **(08 Marks)**

OR

8 a. Design a second order active high pass filter using 741 opamp with cutoff frequency of 12 kHz. **(06 Marks)**

b. What is meant by line regulation and load regulator with respect to IC regulators and mention the characteristics of 3 terminal IC voltage regulators. **(06 Marks)**

c. Design a first order active low pass filter to have cutoff frequency of 1 kHz. Use 741 opamp. **(04 Marks)**

Module-5

9 a. Explain the operation of a Astable multivibrater using 555 timer. **(08 Marks)**

b. Explain operation of PLL with block diagram. **(08 Marks)**

OR

10 a. Explain the operation of a VCO. **(08 Marks)**

b. Explain analog to digital conversion using successive approximation method. **(08 Marks)**

* * * * *

CBCS Scheme

USN | | | | | | | | | | |

15EC46

Fourth Semester B.E. Degree Examination, June/July 2017
Linear Integrated Circuits

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. With a neat circuit diagram, explain basic operational amplifier circuit. **(06 Marks)**

b. Define CMRR of an operational amplifier. A741 op-amp is used in a non-inverting amplifier with a voltage gain of 50. Calculate the typical output voltage that would result from a common mode input with a peak level of 100 mV. **(05 Marks)**

c. Design an averaging circuit to give the average of two inputs which each range from 0.1 V to 1 V. Use 741 op-amp. **(05 Marks)**

OR

2 a. Sketch the circuit of an op-amp difference amplifier circuit. Discuss the working and common mode nulling capability with necessary circuit modification and equations. **(08 Marks)**

b. With a neat circuit diagram, explain direct coupled voltage follower. Also compare voltage follower with emitter follower. **(08 Marks)**

Module-2

3 a. Draw the circuit of a capacitor coupled non-inverting amplifier and explain with necessary design equations. Design a high input impedance capacitor coupled non-inverting amplifier with a gain of 100 and lower cut off frequency of 100 Hz. Assume the load resistance is 2.2 KΩ and input parasitic capacitance as 15 pF. **(10 Marks)**

b. Design a capacitor coupled inverting amplifier for a pass band gain of 100, lower cut off frequency of 120 Hz and upper cutoff frequency to be 5 kHz. Use LF353 BIFET opamp and assume load resistance as 2 KΩ. **(06 Marks)**

OR

4 a. Draw the circuit of an instrumentation amplifier and explain. Also show the method of nulling common mode outputs and how dc output voltage can be level shifted. **(09 Marks)**

b. Design a non-saturating precision half wave rectifier to produce a 2 V peak output from a 1 MHz sine wave input with a 0.5 V peak value. Use a bipolar op-amp with a supply voltage of ±15V. **(07 Marks)**

Module-3

5 a. Sketch the circuit of a symmetrical precision clipper and explain with necessary equations and waveforms. Using bipolar opamp design the circuit to clip a 100 kHz sine wave at ±3V level. **(09 Marks)**

b. Explain the working of Weinbridge oscillator with the help of circuit diagram, waveforms and equations. **(07 Marks)**

OR

6 a. Sketch the circuit of fundamental log amplifier and explain its operation. Also derive an expression for its output voltage. Also mention its drawback. **(08 Marks)**

b. With a neat circuit diagram, explain the operation of inverting Schmitt trigger. Using 741 op-amp with a supply of ±12 V, design an inverting Schmitt trigger circuit to have trigger points of UTP = 0 V and LTP = -1 V. **(08 Marks)**

Module-4

7 a. Explain the operation of first order low pass filter with neat circuit diagram, frequency response and design steps. Using a 741 opamp, design a first order active low pass filter to have a cutoff frequency of 2 kHz. **(08 Marks)**

b. Draw the circuit of a single stage band pass filter and explain the operation with necessary design equations. **(08 Marks)**

OR

8 a. Draw the standard representation of 78XX series 3-terminal IC regulator and enumerate the characteristics of this type of regulators. Also define the following performance parameters of a voltage regulator. (i) Line regulation (ii) Load regulation (iii) Ripple rejection **(08 Marks)**

b. With a neat diagram, explain the operation of low voltage regulator using IC723. Design a voltage regulator circuit using LM723 to obtain $V_0 = 5$ V and $I_0 = 2$ A. **(08 Marks)**

Module-5

9 a. With a neat block schematic, explain the operating principle of PLL. Also define (i) Lock-in range (ii) Capture range and (iii) Pull-in time. **(08 Marks)**

b. Explain the working of Flash ADC with necessary diagram. An 8 bit ADC outputs all 1's when $V_i = 2.55$ V. Find its (i) resolution in mV/LSB and (ii) digital output when $V_i = 1.28$ V **(08 Marks)**

OR

10 a. Draw the internal schematic of IC555, configuring it for astable operation and explain with necessary equations and waveforms. **(08 Marks)**

b. With necessary circuit diagram and equations, explain R-2R DAC. What output voltage would be produced by a DAC whose output range is 0 to 10 V and whose input binary number is, (i) 1010 (for 4 bit DAC) (ii) 10111100 (for an 8 bit DAC). **(08 Marks)**

* * * * *